ELECTRONIC DEVICES AND CIRCUITS

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Unit-2

Junction Field Effect Transistor and MOSFET

The Field Effect Transistor (FET)

- In 1945, Shockley had an idea for making a solid state device out of semiconductors.
- He reasoned that a strong electrical field could cause the flow of electricity within a nearby semiconductor.
- He tried to build one, but it didn't work.
- Three years later, Brattain & Bardeen built the first working transistor, the germanium point-contact transistor, which was designed as the junction (sandwich) transistor.
- In 1960 Bell scientist John Atalla developed a new design based on Shockley's original field-effect theories.
- By the late 1960s, manufacturers converted from junction type integrated circuits to field effect devices.

The Field Effect Transistor (FET)

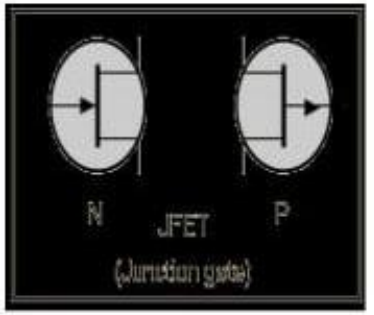
- Field effect devices are those in which current is controlled by the action of an electron field, rather than carrier injection.
- Field-effect transistors are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.
- The FET was known as a “unipolar” transistor.
- The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

The Field Effect Transistor (FET)

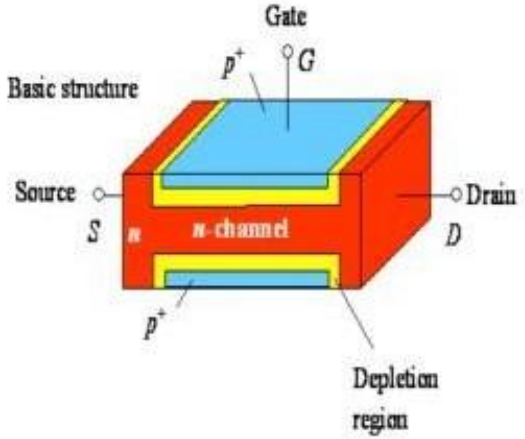
The family of FET devices may be divided into :

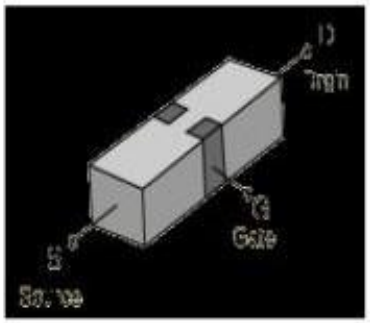
- Junction FET
- Depletion Mode MOSFET
- Enhancement Mode MOSFET

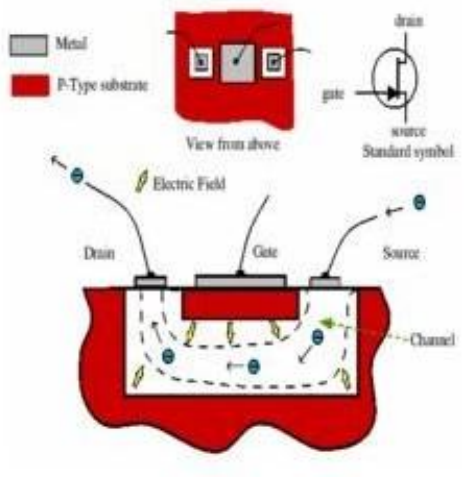
Junction FETs (JFETs



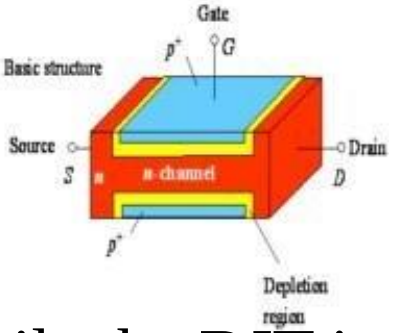
- JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.
- Conducting semiconductor channel between two ohmic contacts - source & drain





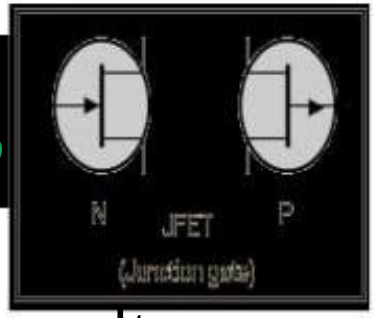


Junction FETs

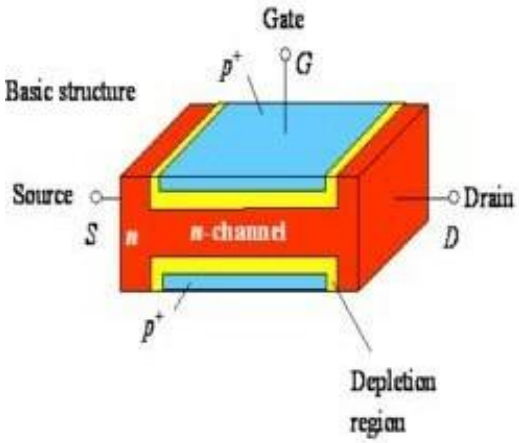


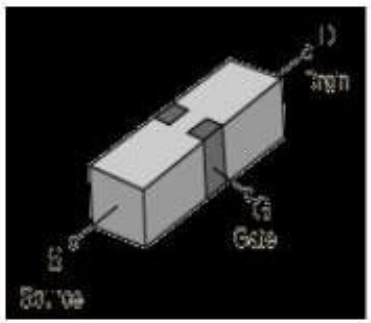
- JFET is a high-input resistance device, while the BJT is comparatively low.
- If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.
- If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.
- N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

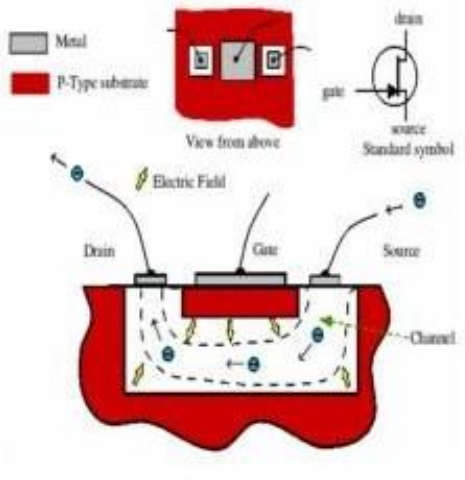
Junction FETs (JFETs



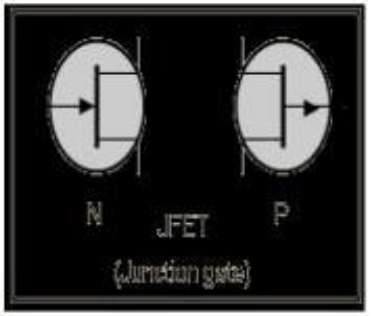
- The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.
- The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.



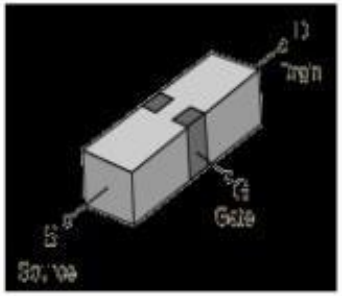


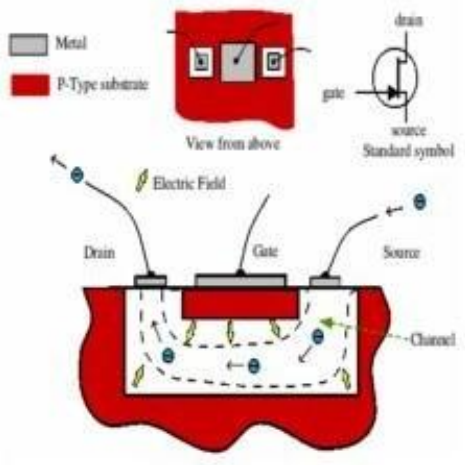


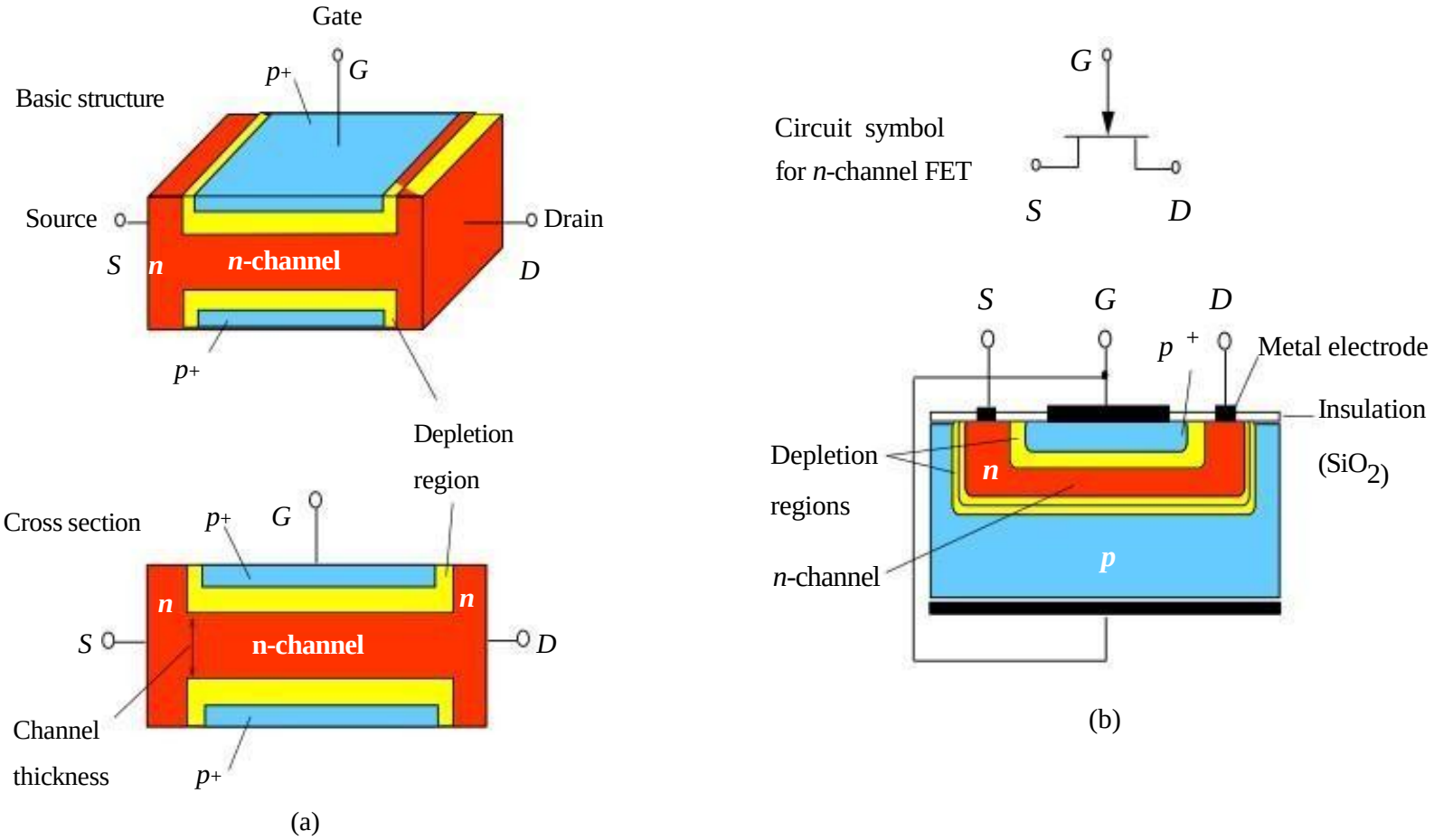
Basic structure of JFE



- In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.
- The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.



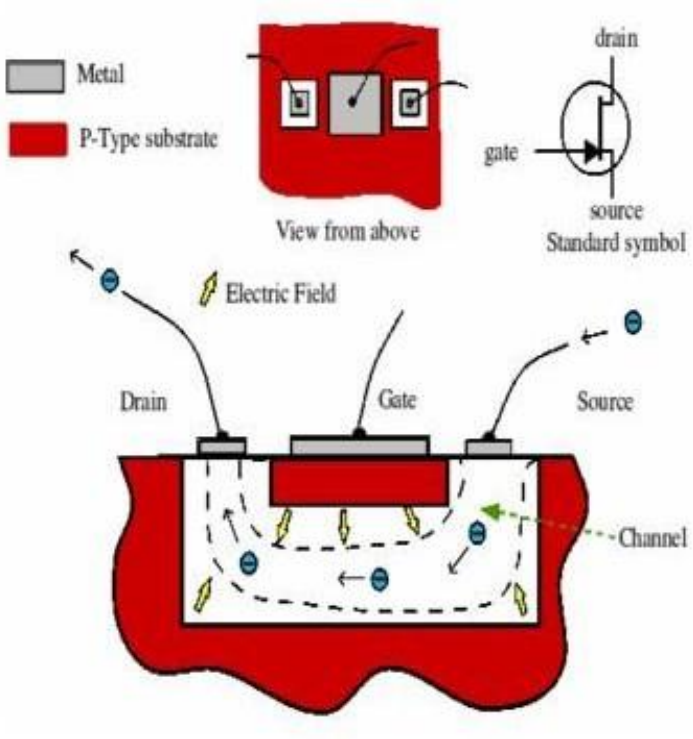




(a)The basic structure of the junction field effect transistor (JFET) with an *n*-channel. The two p^+ regions are electrically connected and form the gate. (b) A simplified sketch of the cross section of a more practical *n*-channel JFET.

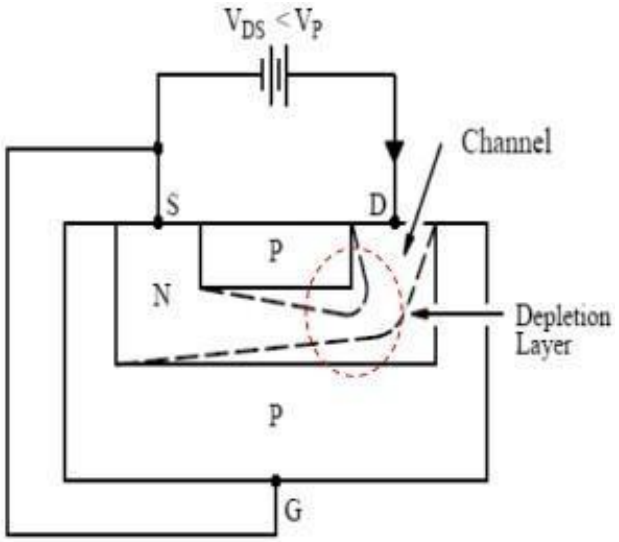
N-channel JFET

- This transistor is made by forming a channel of N-type material in a *P-type substrate*.
- Three wires are then connected to the device.
- One at each end of the channel.
- One connected to the substrate.
- In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side.



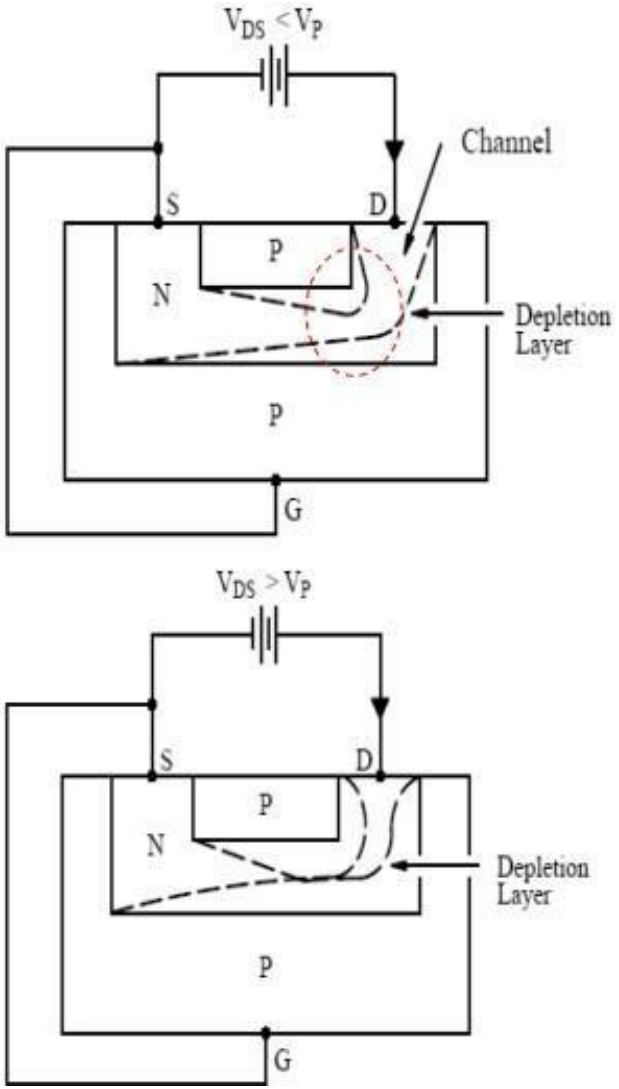
How JFET Function

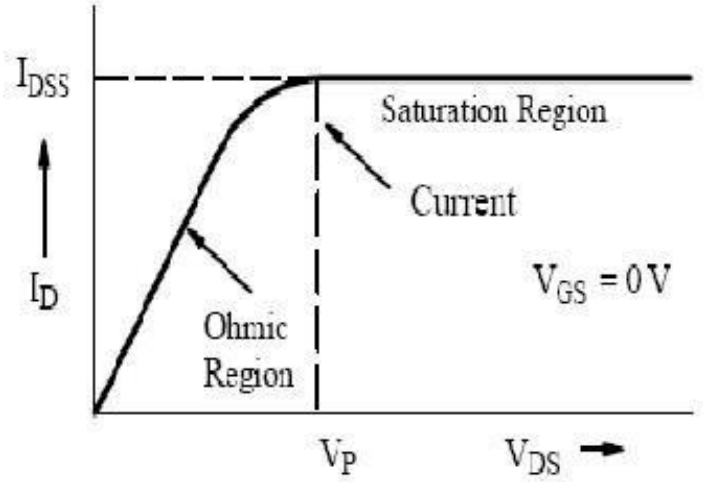
- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection.
- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away.
- The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.



How JFET Function

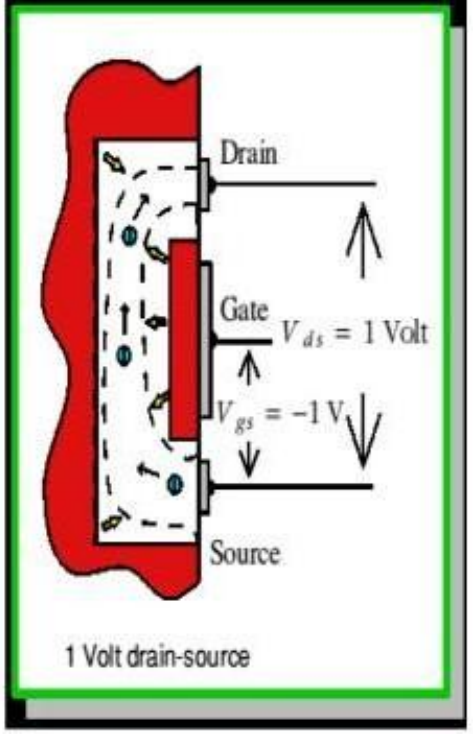
- Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.
- There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel.
- This limiting current is known as I_{DSS} (*Drain-Source current with the gate shorted to the source*).



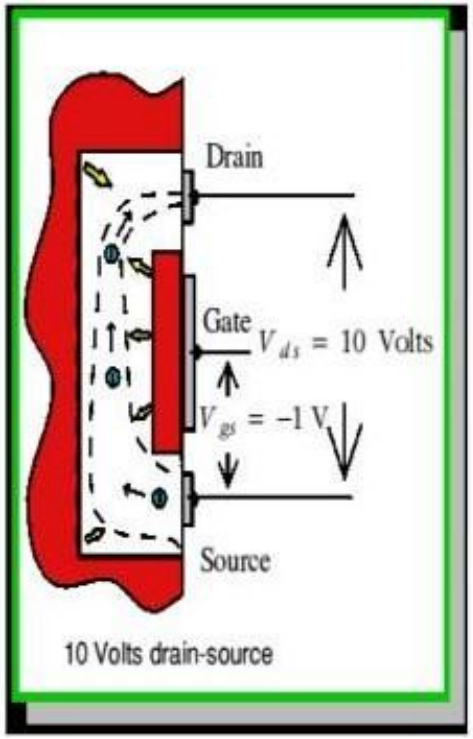


- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases.
- The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.

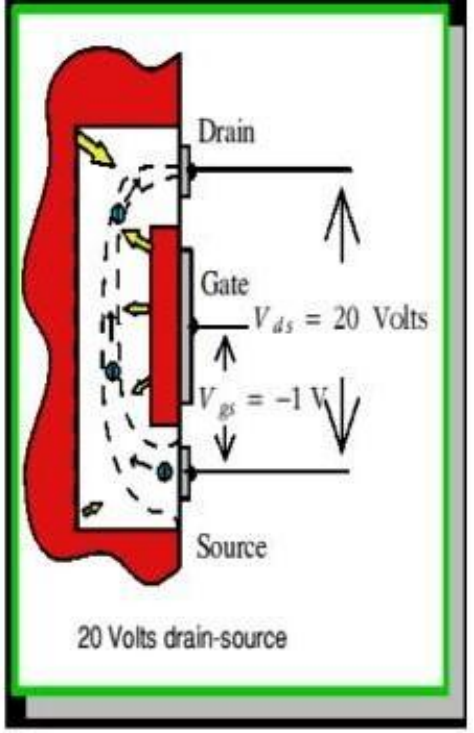
- With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.
- A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (*The drain is 'up'1V from the source potential and the gate is 1V 'down', hence the total difference is 2V.)*
- The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.

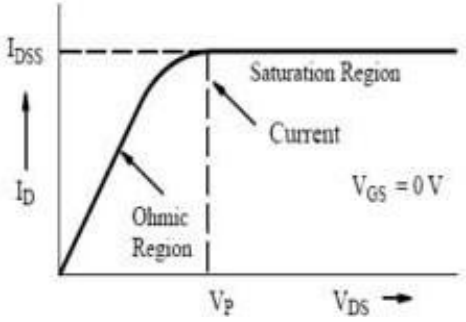


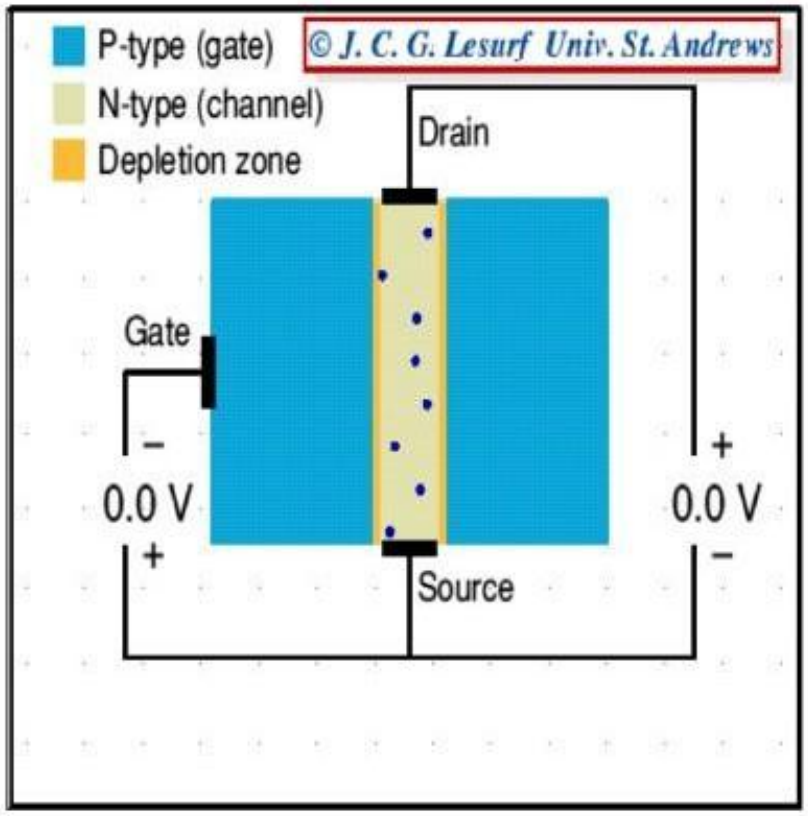
- When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.
- The field across the walls near the drain end is now a lot larger than at the source end.
- As a result the channel near the drain is squeezed down quite a lot.



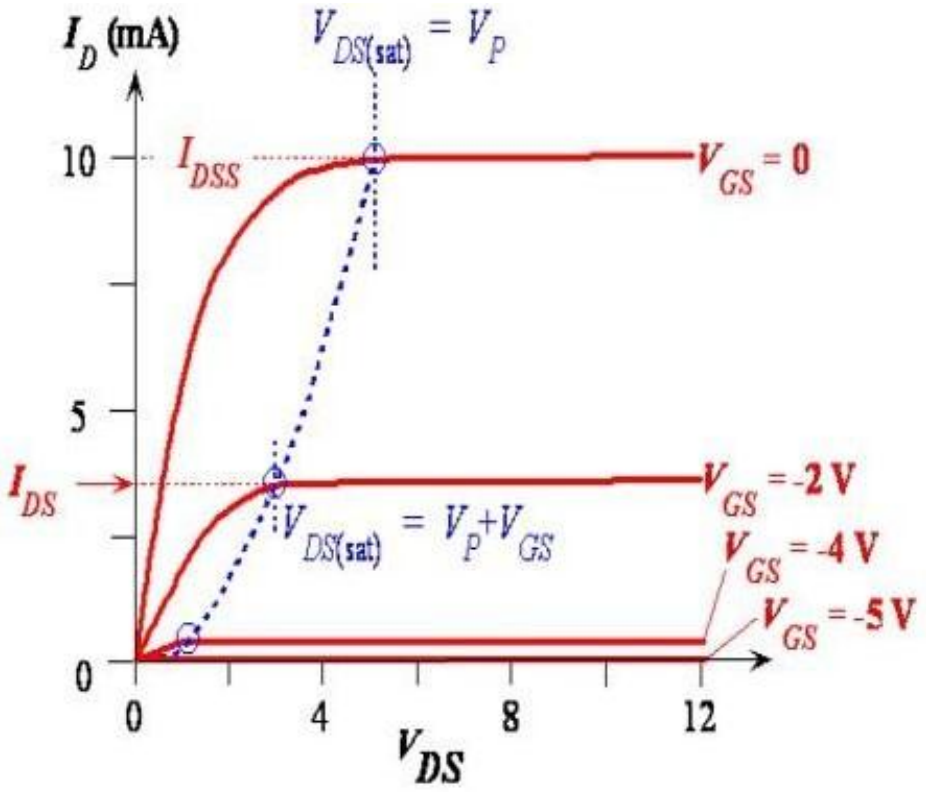
- Increasing the source-drain voltage to 20V squeezes down this end of the channel still more.
- As we increase this voltage we increase the electric field which drives electrons along the open part of the channel.
- However, also squeezes down the channel near the drain end.
- This reduction in the open channel width makes it harder for electrons to pass.
- As a result the drain-source current tends to remain constant when we increase the drain-source voltage.





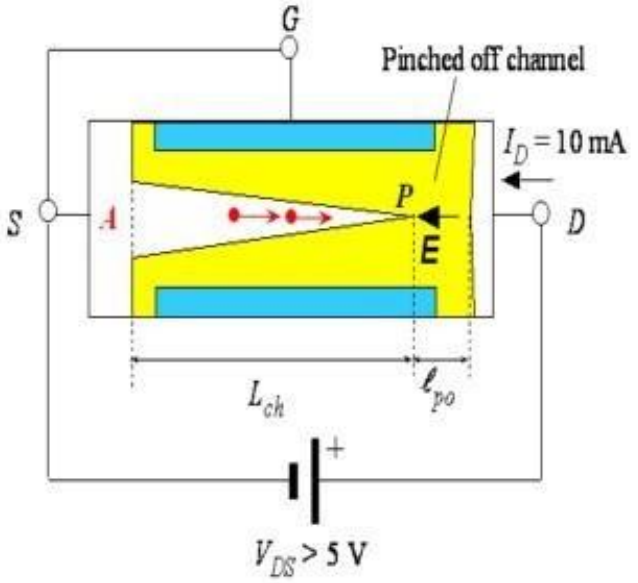

P-type (gate)
N-type (channel)
Depletion zone
© J. C. G. Lesurf Univ. St. Andrews
Drain
Gate
–
0.0 V
+
+
0.0 V
–
Source

- Increasing V_{DS} increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.
  - The resistance of the n-channel, R_{AB} therefore increases with V_{DS}.
  - The drain current: $I_{DS} = V_{DS}/R_{AB}$
  - I_D versus V_{DS} exhibits a sub linear behavior, see figure for $V_{DS} < 5V$.
  - The pinch-off voltage, V_P is the magnitude of reverse bias needed across the p^+n junction to make them just touch at the drain end.
  - Since actual bias voltage across p^+n junction at drain end is V_{GD}, the pinch-off occur whenever: $V_{GD} = -V_P$.



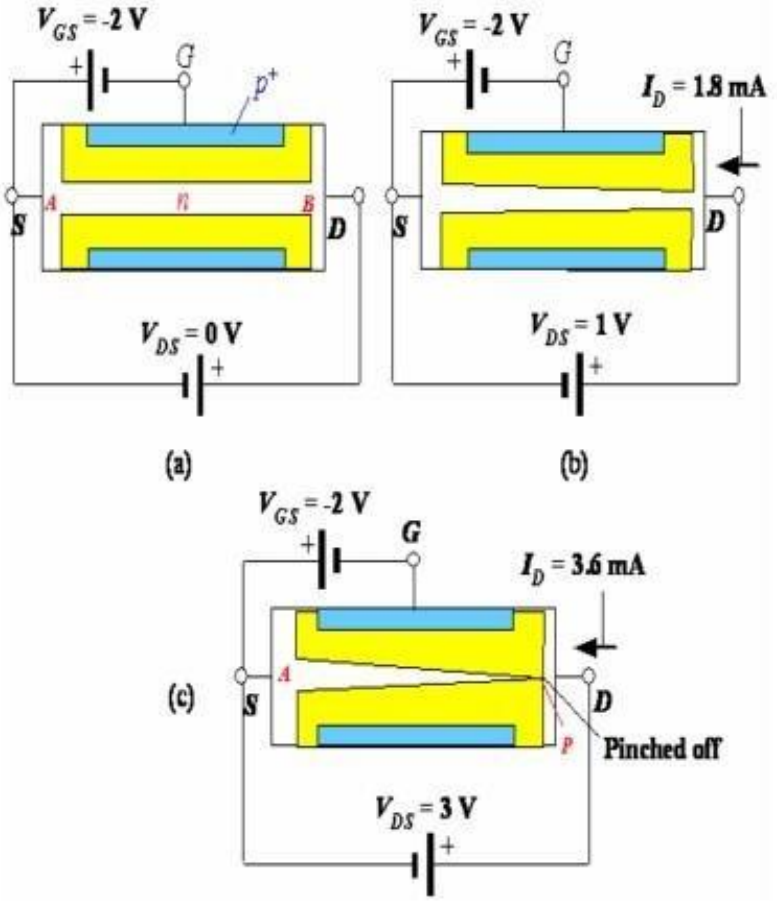
Typical I_D vs V_{DS} characteristics of a JFET for various fixed gate voltages V_{GS}.

- Beyond $V_{DS} = V_P$, there is a short pinch-off channel of length, ℓ_{po}.
- As V_{DS} increases, most of additional voltage simply drops across as this region is depleted of carriers and hence highly resistive.
- Voltage drop across channel length, L_{ch} remain as V_P.
- Beyond pinch-off then $I_D = V_P/R_{AP}$ ($V_{DS}>V_P$).



The pinched-off channel and conduction for $V_{DS} > V_P$ (=5 V).

- What happen when negative voltage, says V_{GS} = -2V, is applied to gate with respect to source (with V_{DS}=0).
- The p^+n junction are now reverse biased from the start, the channel is narrower, and channel resistance is now larger than in the V_{GS} = 0 case.



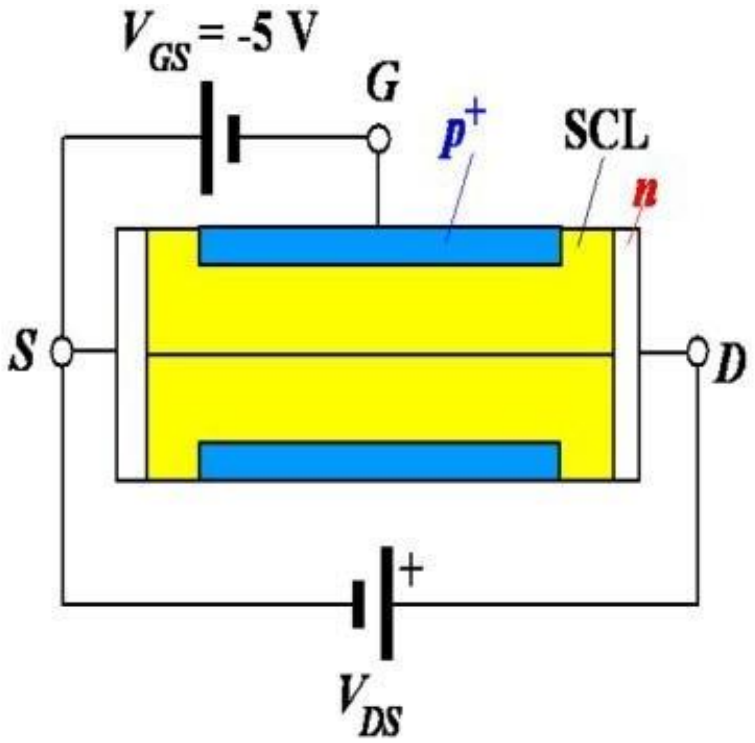
(a) The JFET with a negative V_{GS} voltage has a narrower n-channel at the start. (b) Compared to the V_{GS} = 0 case, the same V_{DS} gives less I_D as the channel is narrower. (c) The channel is pinched off at V_{DS} = 3 V sooner than the V_{GS} = 0 case where it was V_{DS} = 5 V.

- The drain current that flows when a small V_{DS} applied (Fig b) is now smaller than in V_{GS}= 0 case.
- Applied V_{DS}= 3 V to pinch-off the channel (Fig c).
- When V_{DS}= 3V, V_{GD} across $p^{+}n$ junction at drain end is -5V, which is $-V_P$, so channel becomes pinch-off.
- Beyond pinch-off, I_D is nearly saturated just as in the V_{GS}=0 case.
- Pinch-off occurs at $V_{DS}= V_{DS(sat)}$, $V_{DS(sat)}= V_P+V_{GS}$, where V_{GS} is -ve voltage (reducing V_P).
- For $V_{DS}>V_{D(SAT)}$, I_D becomes nearly saturated at value as I_{DS}.

- Beyond pinch-of, with -ve V_{GS}, I_{DS} is

$$I_D \approx I_{DS} \approx \frac{V_{DS(sat)}}{R_{AP}(V_{GS})} = \frac{V_P + V_{GS}}{R_{AP}(V_{GS})}, \quad V_{DS} > V_{DS(sat)}$$

- Where $R_{AP}(V_{GS})$ is the effective resistance of the conducting n-channel from A to P, which depends on channel thickness and hence V_{GS}.
- When $V_{GS} = -V_P = -5V$ with $V_{DS} = 0$, the two depletion layers touch over the entire channel length and the whole channel is closed.
- The channel said to be off.



When V_{GS} = -5 V the depletion layers close the whole channel from the start, at V_{DS} = 0. As V_{DS} is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.

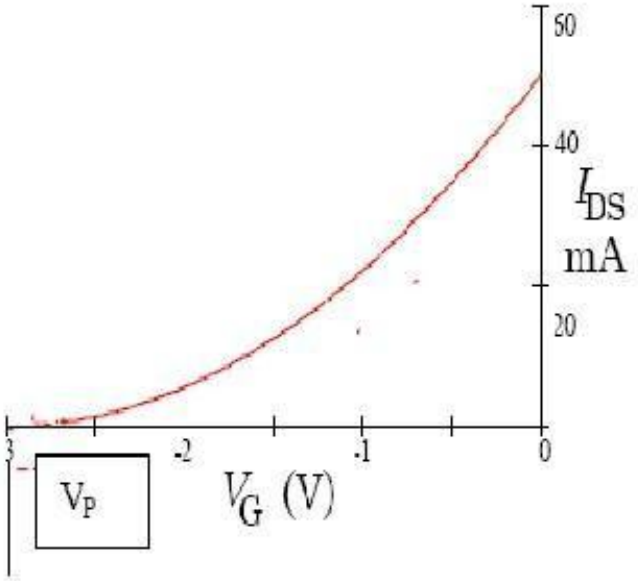
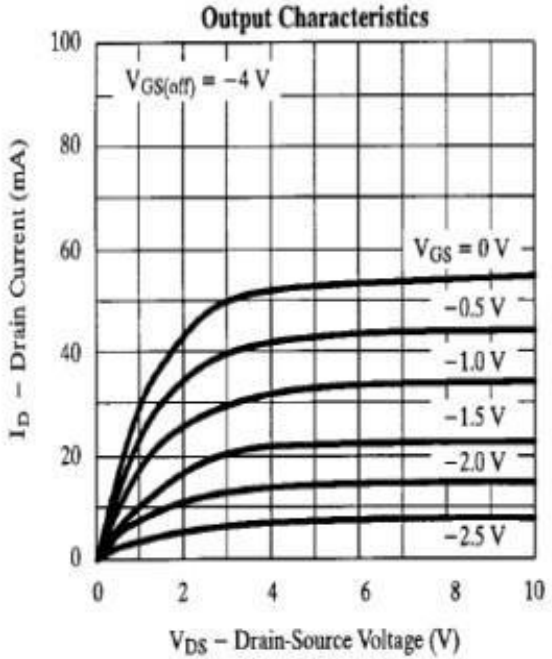
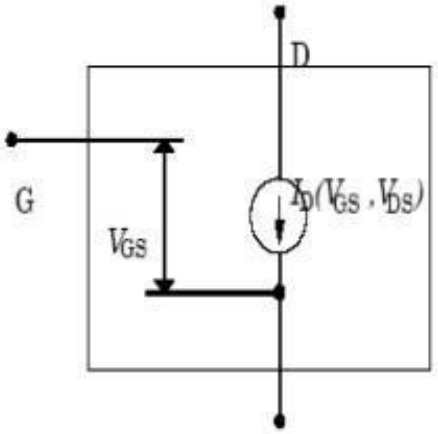


Figure 1: JFET Transfer Characteristic



The source current also depends on the drain source voltage.

A more useful JFET model replaces the variable resistor with a variable current source whose current depends on the gate voltage V_{GS} and the drain-source voltage, V_{DS}.

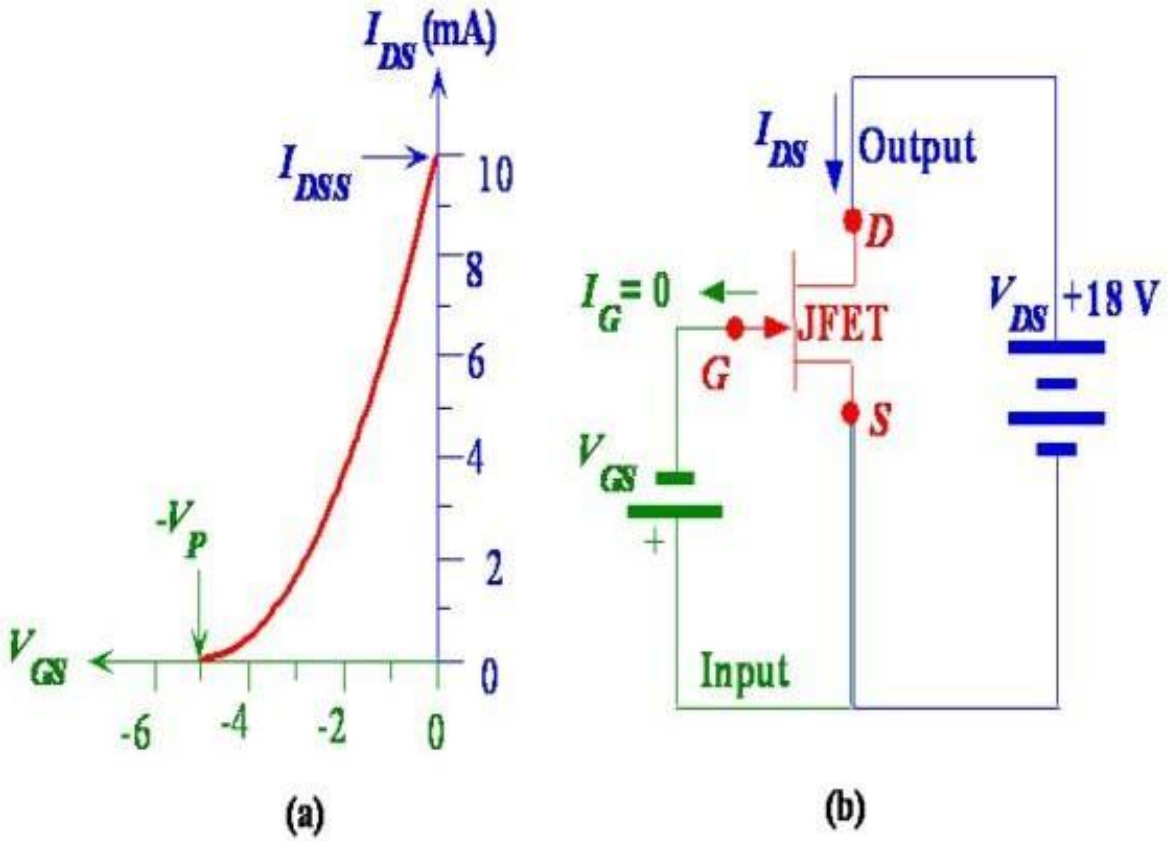


The drain-source current is largest when the gate-source voltage V_{GS} is zero, typically about 50mA. As V_{GS} is made negative, the current decreases. When the gate-source voltage V_{GS} reaches a critical value called the gate-source pinch off voltage V_S, the drain current I_D is cutoff entirely; no current flows. The value of V_S depends on the particular type of JFET (and even varies substantially between JFETs of the same type), but is typically around –4V. As V_{GS} is raised towards 0V, current I_D starts to flow. A typical plot of the current vs. gate voltage is shown in Fig. 1 below. Simple models of JFET performance predict that the curve will be parabolic, but actual devices may differ substantially from this prediction.

- There is a convenient relationship between I_{DS} and V_{GS}.
- Beyond pinch-off

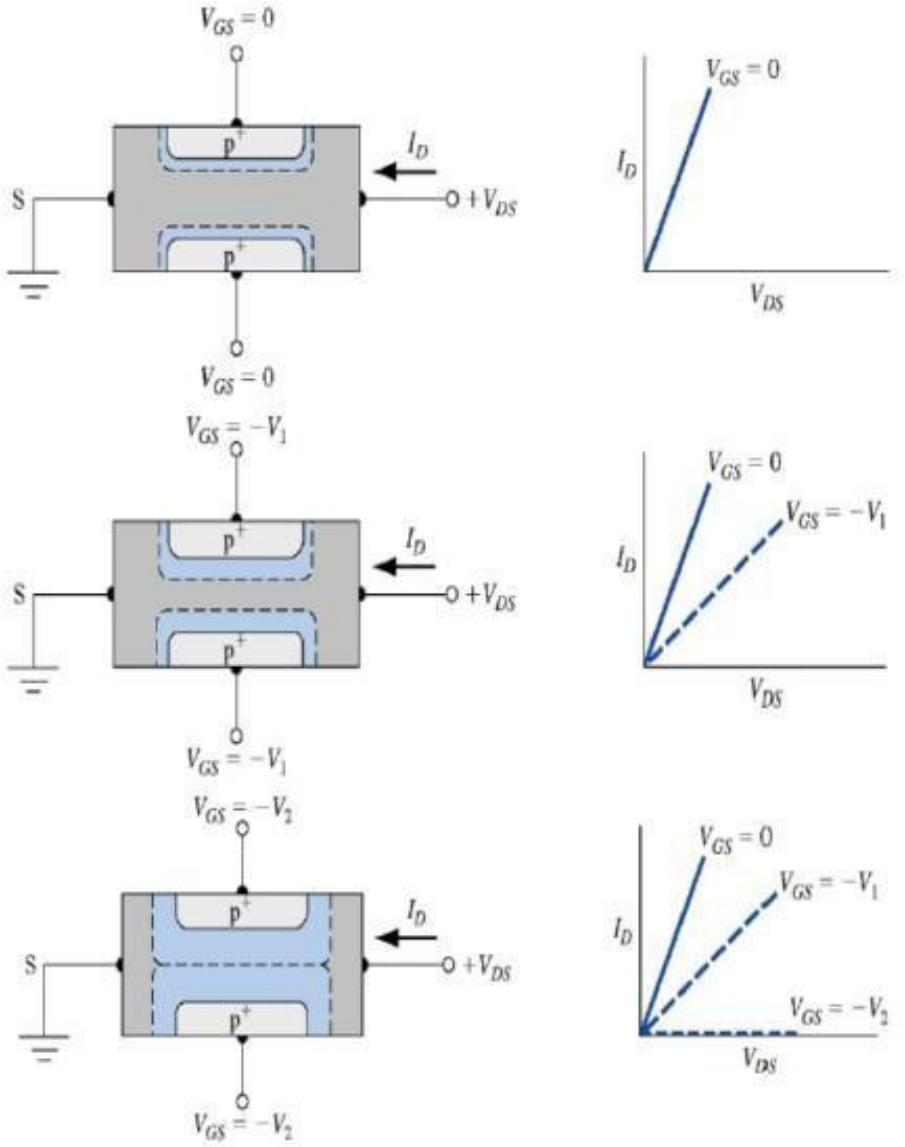
$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_{SG(off)}}\right)^2$$

- Where I_{DSS} is drain current when $V_{GS}= 0$ and $V_{GS(off)}$ is defined as $-V_P$, that is gate-source voltage that just pinches off the channel.
- The pinch off voltage V_P here is a +ve quantity because it was introduced through $V_{DS(sat)}$.
- $V_{GS(off)}$ however is negative, $-V_P$.



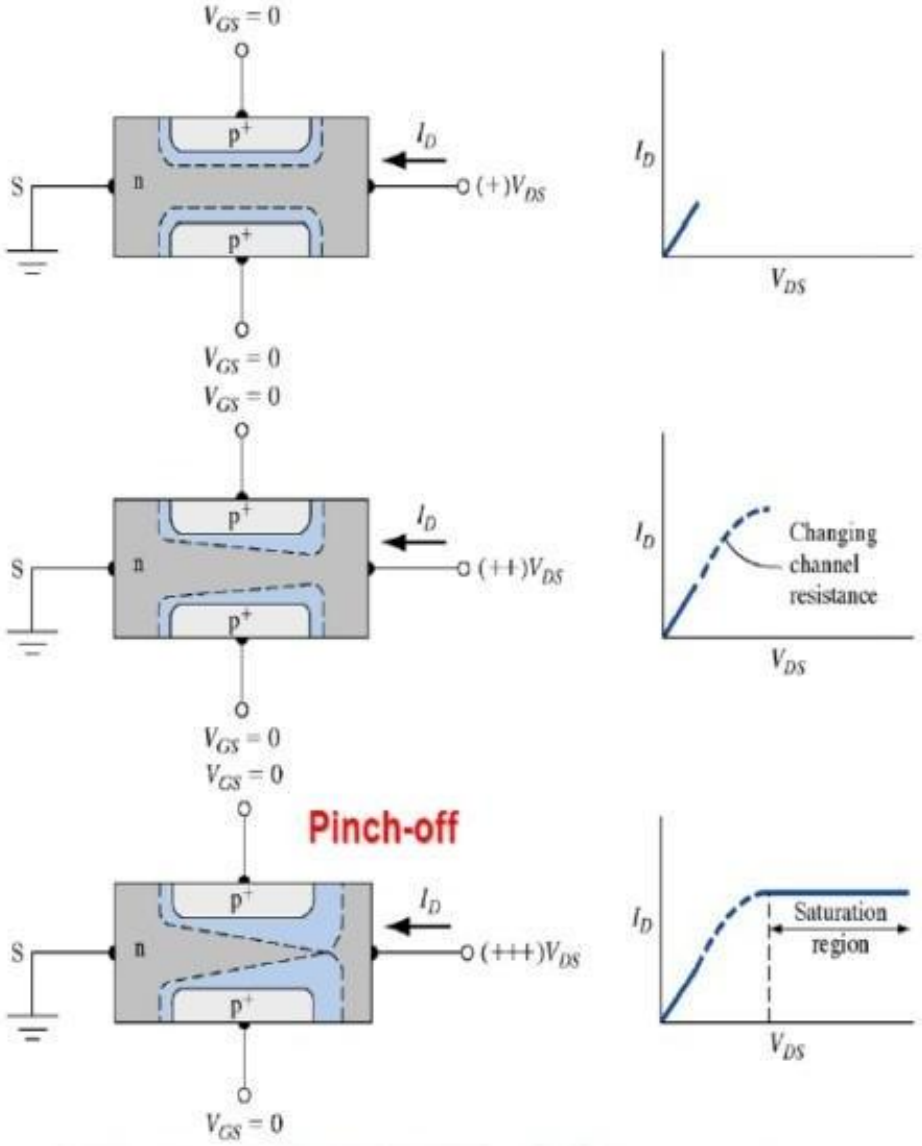
(a) Typical I_{DS} vs V_{GS} characteristics of a JFET (b).
The *DC* circuit in which V_{GS} in the gate-source circuit (input) controls the drain current I_{DS} in the drain-source (output) circuit in which V_{DS} is kept constant and large ($V_{DS} > V_P$).

I-V characteristics



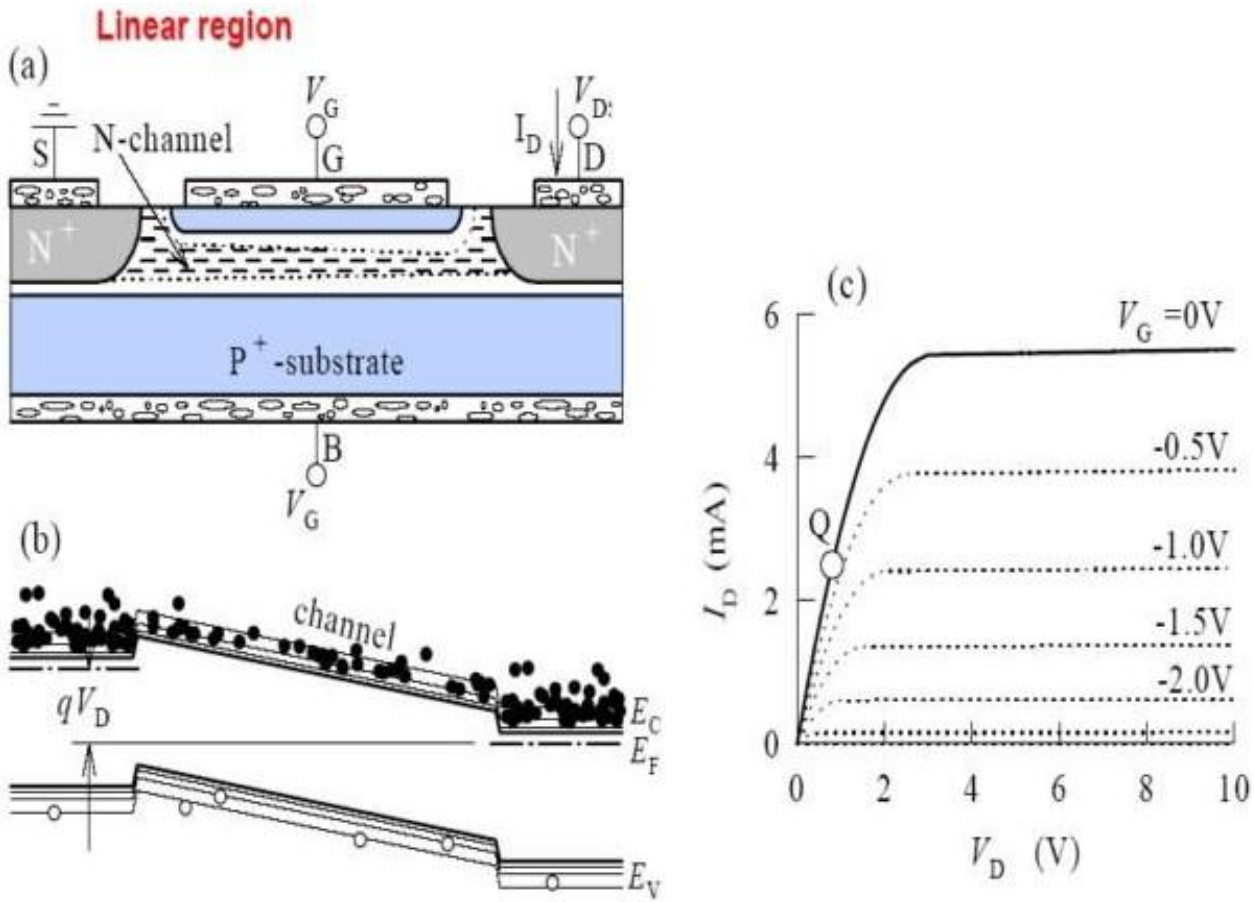
V_G controls the channel width → V_G control I_d

I-V characteristics



After pinch-off: $I_D \neq f(V_D)$; $I_D = f(V_G)$ - current source

JFET: I-V characteristics



The transconductance curve

- The process for plotting transconductance curve for a given JFET:
- Plot a point that corresponds to value of $V_{GS(off)}$.
- Plot that corresponds to value of I_{DSS}.
- Select 3 or more values of V_{GS} between 0 V and $V_{GS(off)}$. For value of V_{GS}, determine the corresponding value of I_D from

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- Plot the point from (3) and connect all the plotted point with a smooth curve.

Example: Plot the transconductance curve for a JFET with $V_{GS(off)} = -6$ V and $I_{DSS} = 3$mA.

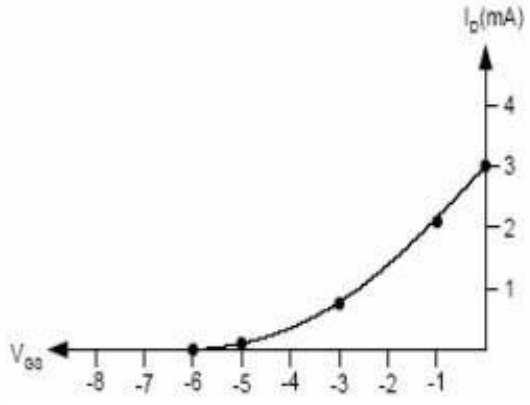
At $V_{GS(off)} = -6$ V , $I_D = 0$.

At $I_{DSS} = 3$ mA , $V_{GS} = 0$.

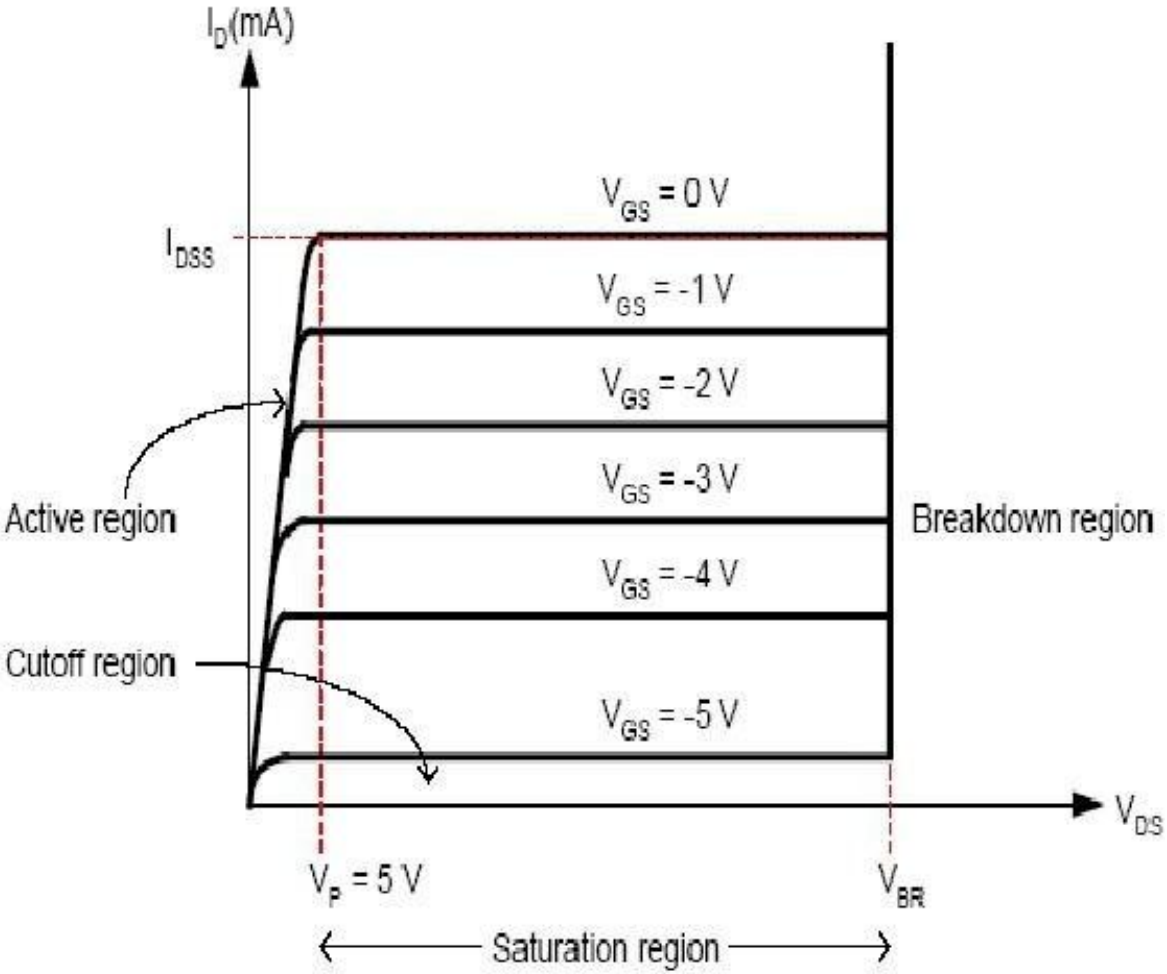
At $V_{GS} = -1$ V , $I_D = 2.08$ mA.

At $V_{GS} = -3$ V , $I_D = 0.75$ mA.

At $V_{GS} = -5$ V , $I_D = 0.083$ mA.



- The relationship between V_{GS}, V_{DS} and I_{DSS} is as shown below.

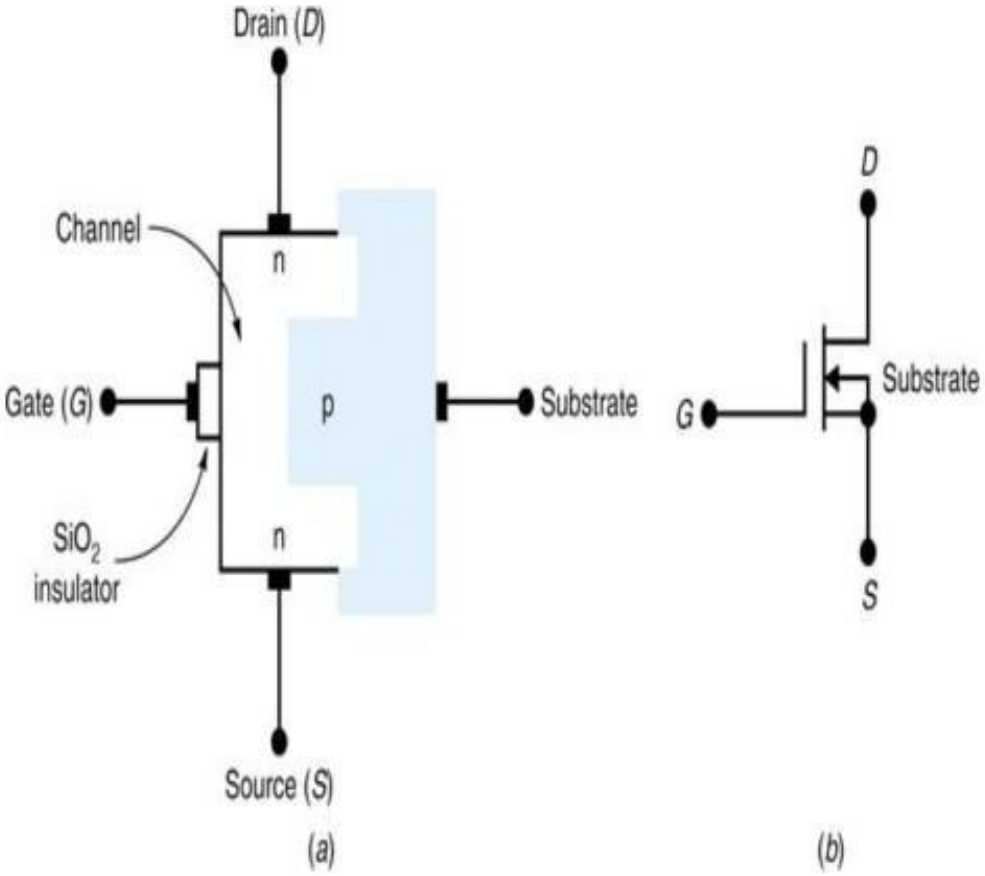


JFET drain curves

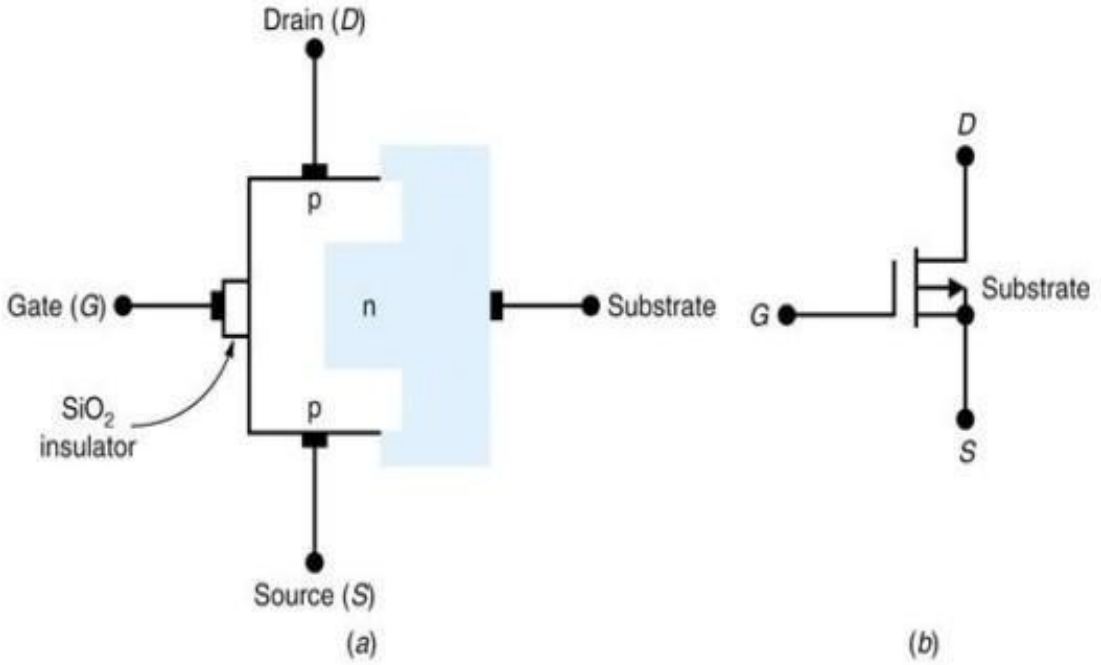
MOSFETs and Their Characteristics

- The **metal-oxide semiconductor** field effect transistor has a gate, source, and drain just like the JFET.
- The drain current in a MOSFET is controlled by the gate-source voltage V_{GS}.
- There are two basic types of MOSFETS: the enhancement-type and the depletion-type.
- The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion-type, a D-MOSFET.
- The MOSFET is also referred to as an IGFET because the gate is insulated from the channel.

MOSFETs and Their Characteristics



MOSFETs and Their Characteristics



MOSFETs and Their Characteristics

Fig. 30-20 (a) shows the construction of an n-channel, enhancement-type MOSFET. The p-type substrate makes contact with the SiO2 insulator. Because of this, there is no channel for conduction between the drain and source terminals.