KCES's College of Engineering & IT Jalgaon Activity Report

Activity Report

Name of The Activity :	TWO week ISTE STTP ON CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN		
Date:	30th Jan 2017 4th Feb. 2017	**Participants profile:**	Faculty

Objective for conducting activity	➢ Update the knowledge OF faculty in VLSI
Methodology	➢ Mannual (using power point presentation)
Out Come	➢ knowledge OF Faculty is updated.

Photos:

HOD

IQAC co-ordinator

Principal

PRINCIPAL
K.C.E.SOCIETY'S
COLLEGE OF ENGG.& INFO
TECHNOLGY, JALGAON

K.C.E. Society's College of Engg. & IT Jalgaon 425001

K.C.E. SOCIETY'S

COLLEGE OF ENGINEERING & IT, JALGAON

Electronics and Telecommunication Engineering Department

Academic Year 2016-17

DATE:08/11/2016

Notice

All faculty members are hereby inform that, TWO-WEEK ISTE STTP ON CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN is organized by E&TC Department in association with IIT Kharagpur, so interested faculty can register your name to workshop coordinator Mr. Pankaj Ranglani on or before 28th November-2016.

HOD

Prof. K.D.Mahajan

Eligibility:

1) He/ she must be a faculty member in the Department of **Electronics and Communication Engineering / Electrical Engineering / Computer Science and Engineering /Instrumentation Engineering /Information Technology /Physics** with basic **VLSI** knowledge/ **Mathematics** with basic **VLSI** knowledge/ **Material Science** with basic **VLSI** knowledge/ related Departments and Centres.
2) B.E. / B. Tech. or equivalent degree holders in the above mentioned disciplines with minimum teaching experience of 2 years and moderate teaching experience in the area of Analog and Digital Circuits.
3) M.E / M.Tech. degree holders in the above mentioned disciplines with minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.
4) Ph.D. degree holders should have a minimum teaching experience of 1 year and moderate teaching experience in the area of Analog and Digital Circuits.

Who may benefit:

The workshop is likely to benefit regular/visiting faculty colleagues who are teaching subjects like VLSI Design, Fundamentals of Radio Frequency Engineering, Design and Implementation of Mixed Signal Circuits and Systems, Design and Analysis of Radio Frequency Integrated Circuits, Mixed Signal and RFIC Design, Analog Front-End Design, Digital VLSI Circuits, VLSI Architecture for Video Processing, etc.

Note:

Please note that this ISTE STTP is conducted under the CEP IIT Kharagpur. Live recording of the course and other created contents will be released under Open Source through a portal. The recorded CD/DVD of the course lectures will be available for distribution, at cost, to any individual or institution. All participants are required to sign an undertaking for such release of contents contributed by them during and after the STTP. The recognition and citation will naturally be made for all contributors.

Course Fee:

This ISTE STTP on 'CMOS, Mixed Signal and Radio Frequency VLSI Design' is funded by the National Mission on Education through ICT (MHRD, Government of India), therefore there is no course fee for participation.

How to Apply:

Those willing to attend this course should register online.

Online Registration link:

http://www.nmeict.iitkgp.ernet.in/vlsidmain.php

Address for Communication:
Admin Team,
Project "T10KT", IIT Kharagpur
Vikramshila Building, ground floor of Kalidas Auditorium
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Remote Center Coordinator
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Workshop Coordinator
Mr. Pankaj Ranglani
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pbranglani@gmail.com

Remote Center Identification Number
(RCID): 1090

College Details:

K.C.E Society's
COLLEGE OF ENGINEERING AND \ INFORMATION TECHNOLOGY, JALGAON
COET Campus, Behind D.I.C., N.
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coeit.inquiry@gmail.com

TWO-WEEK ISTE STTP ON CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN

National Mission on Education through ICT
(MHRD, Govt. of India)

30th January, 2017 to 4th February, 2017

Indian Institute of Technology
Kharagpur 721302
India

Khandesh College Education Society's (Estd.1944)
COLLEGE OF ENGINEERING & INFORMATION TEHNOLOGY
Jalgaon - 425001, Dist. Jalgaon (M.S)

Introduction:

IIT Kharagpur and IIT Bombay are working together with Engineering Colleges of India to enhance the teaching skills of our faculty colleagues in core Engineering and Science subjects by conducting ISTE Short Term Training Programmes (STTPs) under Train Ten Thousand Teachers (T10KT) project using 353 established remote centers across India. Participating teachers attend live lectures at a remote center close to their own college, and also attend tutorial and lab sessions conducted in the same centers. The lecture transmission and live interaction takes place in distance mode using A-VIEW technology through Internet at the selected remote centers across the country.Since December 2009, a number of two-week ISTE STTPs were conducted on various Engineering subjects. We have reached out to more than 1,00,000 teachers and helped them to enhance their teaching skills in these subjects.

In order to run these STTP at selected remote centers, we invite expert faculty members from various remote centres to a five-day Coordinators' training programme held at IIT Kharagpur or at IIT Bombay, at least two months before the main STTP. The trained Coordinators then act as Workshop Coordinators during the main STTP liaising between the participants at their Remote Centers and IIT Kharagpur / IIT Bombay from where the interactive lectures are transmitted live. During the main STTP, the workshop Coordinator at every center supervises the tutorials and laboratories. All the lectures and tutorial sessions are recorded at IIT Kharagpur or at IIT Bombay. The final edited audio-visual contents, along with other course material are released under Open Source. The contents can be freely used later by all teachers, students and other learners.

In the backdrop of the success of these STTPs, we now announce another 6 day ISTE STTP on **"CMOS, Mixed Signal and Radio Frequency VLSI Design"** during January 30 - February 4, 2017 under **Blended MOOCs** (Massive Open Online Courses) model.

Here,

1. The participating teachers will complete the equivalent of two-week full time work online, spread over 6 physical weeks where video lectures and assignments will be uploaded beforehand.
2. After completing the online assignments spread over 4 to 5 weeks the participants will assemble at the selected Remote Centers for 6 days face to face interaction and lecture sessions through A-VIEW and will complete team assignments, tutorials, quizzes etc.
3. Offline assignments will be uploaded and the participants will have to complete these assignments within a stipulated time.
4. There will also be a system of students' feedback in the Main STTP.

The above proposed model is tentative and subjected to minor changes

Course Justification:

Design, analysis and implementation of CMOS Mixed Signal and RFIC are attractive topics both in academia and Industry. CMOS RFIC design is a challenging and critical engineering task particularly in the arena of deep sub-micron technology. There is a strong demand of manpower having thorough knowledge and hands on experiences in VLSI design using state of the art EDA tools. The course will focus on those issues along with case studies.

Course Domain:

Electronics Engineering/Electrical Engineering/Computer Science and Engineering

Expectation from the Participants:

It is assumed that before taking the courses, the participants are familiar with introduction to electronic circuit components, signal and system theory, VLSI design technology and basic CAD flow for electronic system.

Course Objective:

Design and implementation methodology of :

1. **Analog front end for sensor interface:** Instrumentation Amplifier (IA), chopper, Variable Gain Amplifier (VGA)
2. **Data converters:** SAR & pipelined ADC.
3. **Digital VLSI:** a) Static MOS gate circuits b) High-Speed CMOS Logic Design c) Transfer Gate and Dynamic Logic Design d) VLSI architectures for video processing
4. **RF circuits:** Introduction to RFIC design.
5. **Design and implementation of typical RF Tx-Rx sub-components:** (a) Low Noise Amplifier (LNA) (b) Mixer c) Frequency synthesizer (d) Power amplifier (e) Lay out and chip level integration

Design Methodology:

From pen-paper design of various mixed signal/RF circuit blocks to schematic level implementation and then sub-sequent physical design, post-layout synthesis and simulation.

Course Modules:

1. **Radio Frequency Integrated Circuits (RFIC) :**

   Module-A Fundamental of RFIC design, How RF design alters from traditional analog design. Various commercial protocols, basic Tx-Rx Architecture.

   Module-B Various performance parameters, Noise.

   Module C Design of LNA, VCO, Mixer and frequency synthesizer, Power amplifier, High speed I/O(SERDES), layout of RF circuit design.

2. **Mixed Signal Blocks :**

   i) Digital VLSI Design: High-Speed CMOS Logic, Transfer Gate and Dynamic Logic

   a) Basics of video processing

   b) VLSI Architectures for video processing

   ii) Analog Design: Analog front-end electronics (AFE), SAR ADC, Pipelined ADC.

Duration and Venue:

The duration of the STTP will be six working days. It will start on **Monday 30th January, 2017 at 9:30 AM** and will end on **Saturday 4th February, 2017**.The participants must report to the respective remote centres by 8:00 AM on 30th January, 2017.

Venue: 206 remote centers located in different parts of the country. The list of participating remote centers is given along with online application form.

Teaching Faculty:

1. Prof. T. K. Bhattacharya, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email: tkb@ece.iitkgp.ernet.in
2. Prof. Indrajit Chakrabarti, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email : indrajit@ece.iitkgp.ernet.in
3. Dr. Mrigank Sharad, Department of Electronics & Electrical Communication Engineering. IIT Kharagpur, Email : mrigank@ece.iitkgp.ernet.in

Gmail

Rahulkumar Patel <rprahulpatel850@gmail.com>

STTP on "CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN"

Pankaj Ranglani <pbranglani@gmail.com>
Tue, Nov 8, 2016 at 9:55 AM
To: shah.paresh@sscoetjalgaon.ac.in, thakre.prashant@sscoetjalgaon.ac.in, pawar.vijay@sscoetjalgaon.ac.in, ansari.mujtahid@sscoetjalgaon.ac.in, shembekar.suhas@sscoetjalgaon.ac.in, patil.dhanesh@sscoetjalgaon.ac.in, mahajan.nilesh@sscoetjalgaon.ac.in, swapnilbhuskute2408@gmail.com, bholeneha21@gmail.com, lokeshlondhe2010@gmail.com, akshata403@gmail.com, suralkar.shekhar@sscoetjalgaon.ac.in, deshmukh.manish@sscoetjalgaon.ac.in, adokar.dineshkumar@sscoetjalgaon.ac.in, deshmukh.vijay@sscoetjalgaon.ac.in, kazi.nafis@sscoetjalgaon.ac.in, karode.atul@sscoetjalgaon.ac.in, wani.amol@sscoetjalgaon.ac.in, zope.pankaj@sscoetjalgaon.ac.in, ramteke.surendra@sscoetjalgaon.ac.in, khode.sunil@sscoetjalgaon.ac.in, bari.ashish@sscoetjalgaon.ac.in, patil.dipeeka@sscoetjalgaon.ac.in, deshmukh.mayuri@sscoetjalgaon.ac.in, shanbhag.priyanka@sscoetjalgaon.ac.in, sapkal.akshada@sscoetjalgaon.ac.in, hingonekar.shailendra@sscoetjalgaon.ac.in, santwani.yogesh@sscoetjalgaon.ac.in, paras.kunal@gmail.com, priyankagirase6@gmail.com, charansingh.patil@gmail.com, sagarchavan.etc@gmail.com, sukruti2010@gmail.com, khadkepm@gmail.com, sadik_khan05@yahoo.co.in, madhu.sisodiya13@gmail.com, patil.kiran@sscoetjalgaon.ac.in, nikam.chandrashekhar@sscoetjalgaon.ac.in, patil.mahendra@sscoetjalgaon.ac.in, tmpatil75@rediffmail.com, patil_pankaj_sa@yahoo.com, tnvmahajan@gmail.com, dhande.pawan@gmail.com, dheeraj.pongallu@yahoo.com, mohini10nov@gmail.com, patilpruthvi123@yahoo.in, sur_wani@rediffmail.com, vaishali.rane293@gmail.com, Kalpesh Mahajan <kalpmahajan@gmail.com>, prasadonly1@yahoo.com, Sachin Maheshri <sachinmaheshri@gmail.com>, dipalip16@rediffmail.com, kanchanpatil2893@gmail.com, jayeshrmahajan7@gmail.com, badgujaryogesh1110@gmail.com, patilrv12@gmail.com, rupali1305patilaol@gmail.com, Kirti Mahajan <kirtimhjn@gmail.com>, kishor jadhav <kpj2007@rediffmail.com>, Mukesh Tiwary <mukesh.tiwary007@gmail.com>, Pravin Bhangale <pravinbhangale55@gmail.com>, Hemant Wani <wanihemant1983@gmail.com>, wanihemant1983 <wanihemant1983@yahoo.co.in>, wanihemant1983@rediff.com, Swapnil Patil <swapnilspatil85@gmail.com>, MINAL GADE <minalgade2002@gmail.com>, patel rahul Rajaram <rprahulpatel850@gmail.com>, Sneha Varade <sonu14485@gmail.com>, Madhuri Chaudhari <chaudhari10.madhuri@gmail.com>, Nitin Matkari <matkarinn@gmail.com>, bhushan_aloni@yahoo.com, npardeshi29@gmal.com, bhavnasonawane2010@gmail.com, sonalwaychol@gmail.com, deepakrbonde71@gmail.com, vishu.315@gmail.com, mayur2203@gmail.com, Swapna Bhirud <bhirud.swapna177@gmail.com>, Roshankumar Bhamare <roshankumarbhamare@gmail.com>, pallavipawar511@gmail.com, Sanjay Pawde <pawdesanjay@gmail.com>, mbchaudhari@rediffmail.com, sarita.jain2287@gmail.com, shitalfirke13@gmail.com, manda201992@gmail.com, dbahirrao2011@rediffmail.com, shwetapandey806@gmail.com, minal kolhe <minaltkolhe@gmail.com>, nandini113 <nandini113@yahoo.co.in>, tussharkolhe@gmail.com, harshachavan2025@gmail.com, Priyanshi Borase <priyanshiborase@gmail.com>, Leena Waghulde <waghuldeleena.2008@gmail.com>, zambrerupali@gmail.com, harshatalele19@gmail.com, naval.puja@rediffmail.com, diptivpatil25@gmail.com, patnaik.girish@sscoetjalgaon.ac.in, adhiya.krishnakant@sscoetjalgaon.ac.in, patil.manoj@sscoetjalgaon.ac.in, patil.sandip@sscoetjalgaon.ac.in, patil.nilima@sscoetjalgaon.ac.in, suryawanshi.nitin@sscoetjalgaon.ac.in, borse.yogeshwari@sscoetjalgaon.ac.in, puri.dinesh@sscoetjalgaon.ac.in, patil.shital@sscoetjalgaon.ac.in, sharma.priti@sscoetjalgaon.ac.in, bage.dipak@sscoetjalgaon.ac.in, rajput.satpalsing@sscoetjalgaon.ac.in, bahekar.sushant@sscoetjalgaon.ac.in, waghmare.akash@sscoetjalgaon.ac.in, chaudhari.prachi@sscoetjalgaon.ac.in, tayade.dhanashri@sscoetjalgaon.ac.in, pandey.sweta@sscoetjalgaon.ac.in, nareshdkale123@gmail.com, shrutikaamahajan@gmail.com, shinde.archana@sscoetjalgaon.ac.in, sharmapareshd@gmail.com, kotwal.harshal@sscoetjalgaon.ac.in, patil.pravink@sscoetjalgaon.ac.in

Dear All,

With great contentment and delight we would like to inform you that, **K.C.E.S's College of Engineering & Information Technology (Remote Center Identification Number (RCID) – 1090)**, Jalgaon in association with National Mission on Education ICT (MHRD Government of India) is organizing

Short Term Training Program (STTP)

"CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN"

30th January -04th February 2017

under Train Ten Thousand Teachers (T10KT)

The aim of this STTP is to promote design, analysis and implementation of CMOS mixed signal and RFIC design both in Academics and Industry.

Registration Process:

Please kindly visit the following link for more details:

http://www.nmeict.iitkgp.ernet.in/

http://www.nmeict.iitkgp.ernet.in/vlsidmain.php

http://www.nmeict.iitkgp.ernet.in/regi_coordinator/vlsidmw_instruction.php

Start date of registration : 26th October 2016

Last date of registration : 28th November 2016

There is no course fee as the STTP is funded by National Mission on Education through ICT (MHRD, Government of India).

Course Objective:-

A. **Design and Implementation methodology of:**
   1. **Analog Front End for Sensor Interface:**
      a. Instrumentation Amplifier (IA)
      b. Chopper
      c. Variable Gain Amplifier.
   2. **Data Converters:** SAR & Pipelined ADC.
   3. **Digital VLSI:**

a. Static MOS gate circuits.
b. High Speed CMOS Logic Design.
c. Transfer Gate and Dynamic Logic Design.
d. VLSI architectures for video processing.

4. **RF Circuits:** Introduction to RFIC design.
5. **Design and Implementation of typical RF Tx-Rx sub components:**
   a. Low Noise Amplifier (LNA).
   b. Mixer.
   c. Frequency Synthesizer.
   d. Power Amplifier.
   e. Layout and Chip level Integration.

B. Design Methodology:

From pen-paper design of various mixed signal/RF circuit blocks to schematic level implementation and then su-sequent physical design, post layout synthesis and simulation.

Kindly visit the above links for on line registration and for more information.

The information brochure is attached herewith.

We look forward for your gracious presence.

Kindly share the above information with your colleagues.
Feel free to contact.
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Thanks & Regards

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Assistant Professor
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Khandesh College of Education Society's,
College of Engineering & Information Technology
(K.C.E.S's, C.O.E.I.T), Jalgaon

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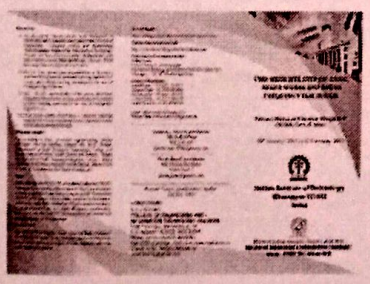
5 attachments



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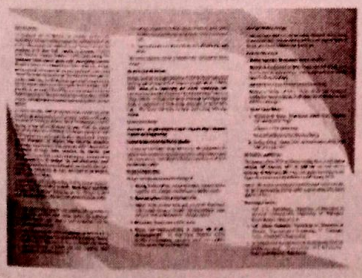

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PermissionLetterGroupForMainWorkshop OnVLSIDesign.docx
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Attendance Sheet for Date : 2020-02-08

One Day Workshop on Arduino without kit on 8 February 2020 is limited to 100 BCs

February 8th, 2020 to February 8th, 2020

Under the National Mission on Education through ICT, MHRD, New Delhi

1000 - K.C.E. Society, COEIT, Jalgaon

Participant			Signature			
S No	Participant ID	Name	Session 1	Session 2	Session 3	Session 4
1	221697	Hemant Wani				
2	221711	Prasad Kulkarni				
3	221736	Mukesh Kumar Tiwari				
4	221755	Sanjay Sugandhi				
5	221779	Pravin Bhangale				